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### (54) Thin film transistor and method of manufacturing it.

(55) A thin film transistor comprises a source area (102) and a drain area (103) which are composed of a silicon thin film to which an impurity which serves as a donor or an acceptor is added, a channel area (104) composed of the silicon thin film formed between said source area and said drain area in contact with said source area and said drain area, a gate insulation film (107) formed in such a manner as to cover said source area, said drain area, and said channel area, and a gate electrode (108) disposed on said gate insulation film. The gate electrode does not overlap said source area or said drain area, allowing a high ON/OFF ratio to be realized. Described are various methods for producing such a thin film transistor.

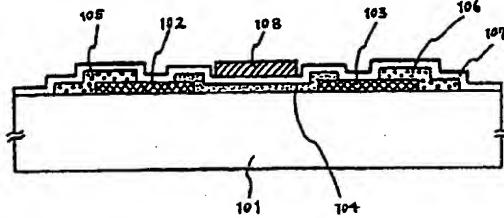


FIG. 1

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The present invention relates to a thin film transistor which is particularly suitable for use in active matrix type liquid crystal devices, image sensors, three-dimensional integrated circuits or the like.

An example of the construction of a conventional thin film transistor will be explained with reference to Fig. 2. Fig. 2 is a cross-sectional view of the construction in the direction of a channel. A source area 202 and a drain area 203, which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, to which an impurity which serves as a donor or an acceptor is added, are formed on an insulating substrate 201 of glass, quartz, sapphire or the like. A channel area 204 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of an end of the source area 202 and the top side of an end of the drain area 203 in such a manner as to connect these two areas. A source electrode 205 composed of a metal, a transparent electrically-conductive film, etc. is disposed so as to be in contact with the source area 202, and a drain electrode 206 composed of a metal, a transparent electrically-conductive film, etc. is disposed so as to be in contact with the drain area 203. All of the above is coated with a gate insulation film 207 such as a silicon oxide film, etc. A gate electrode 208 composed of a metal, a transparent electrically-conductive film, etc. is disposed in such a manner as to cover both the source area 202 and the drain area 203, or at least cover a part of each of them. The gate insulation film 207 also serves as an interlayer insulation film for maintaining the insulation among interconnections.

The above-described prior art suffers from the following problems.

Fig. 3 is a graph showing an example of the characteristics of an N-channel thin film transistor having the construction illustrated in Fig. 2. The horizontal axis indicates the gate voltage  $V_{GS}$ , the vertical line indicates logarithmic values of the drain current  $I_D$ . In this example, a current that flows between the source and the drain when the transistor is in an OFF-state is denoted as  $I_{OFF}$ ; a current that flows between the source and the drain when the transistor is in an ON-state is denoted as  $I_{ON}$ . A transistor having characteristics such that the ON-current is large and the OFF-current is small, or in other words, characteristics of a high ON/OFF ratio ( $I_{OFF}/I_{ON}$ ), is preferable. However, generally, if the ON-current is increased, the OFF-current has the tendency to increase also. This fact poses a problem, particularly when an attempt is made to realize an integrated driver type liquid crystal device. That is, it is required that transistors used in the pixel section of a liquid crystal device have

characteristics of a low OFF-current, whereas it is required that transistors used in the peripheral circuits have characteristics of a high ON-current in order to allow a high speed operation.

5 The present invention is intended to solve the above-mentioned problems and to provide a thin film transistor having characteristics of a high ON/OFF ratio ( $I_{OFF}/I_{ON}$ ), and a method for manufacturing such a transistor.

10 The general solution to this object as well as specific embodiments of the invention are defined in the claims.

15 These and other objects, features and advantages of the present invention will become clear from the following description of preferred embodiments of the present invention with reference to the accompanying drawings, in which:

20 Fig. 1 Is a cross-sectional view showing an example of the construction of a thin film transistor according to the present invention;

Fig. 2 Is a cross-sectional view showing an example of the construction of a conventional thin film transistor;

25 Fig. 3 Is a graph showing the characteristics of the conventional thin film transistor;

Figs. 4(a) to 4(d) are cross-sectional views showing process steps of an embodiment in which a thin film transistor having a structure which is known as a means for reducing the OFF-current is realized;

30 Fig. 5 Is a graph showing the characteristics of the thin film transistor according to the present invention;

Figs. 6(a) to 6(c), Figs. 7(a) to 7(c), Figs. 8(a) to 8(c), Figs. 9(a) to 9(c), Figs. 10(a) to 10(d), Figs. 11(a) to 11(d), Figs. 12(a) to 12(d), Figs. 13(a) to 13(d), Figs. 14(a) to 14(c), and Figs. 15(a) to 15(c) are cross-sectional views showing process steps of embodiments of the manufacturing method according to the present invention; and

35 Fig. 16 Is a cross-sectional view showing an example of the construction of the thin film transistor.

40 The thin film transistor of the present invention is characterized in that a gate electrode does not overlap a source area and a drain area, that is, it is formed in a so-called offset structure.

45 As can be understood from the characteristics of a conventional thin film transistor shown in Fig. 3, the OFF-current depends upon the gate voltage, and more particularly, depends upon the voltage between the gate and the drain. The value of the

OFF-current becomes a minimum in the vicinity of a gate voltage of 0 V if an impurity used to control a threshold value is not added to the channel section. That is, it can be said that if the electric field applied between the gate and the drain is reduced, the OFF-current can be reduced. As regards a method of reducing the electric field applied to the gate and the drain, a method of lowering the impurity concentration of the drain end is known. This method will be explained with reference to Fig. 4.

A pattern 402 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is formed on an insulating substrate 401 of glass, quartz, sapphire or the like. Next, all of the above is coated with a gate insulation film 403 such as a silicon oxide film, etc. Formed thereon is a gate electrode 404 composed of a metal, a transparent electrically-conductive film, a polycrystalline silicon film to which an impurity which serves as a donor or an acceptor is added, etc. (See Fig. 4(a)).

Next, by adding, for example, approximately  $1 \times 10^{14} \text{ cm}^{-2}$  of the impurities which serve as a donor or an acceptor by ion implantation, a low-concentration source area 405 and a low-concentration drain area 406 are formed self-aligned with respect to the gate electrode 404 (See Fig. 4(b)).

Then, after an insulation film 407 of, for example, silicon oxide, has been formed on all of the above, this insulation film 407 is etched by anisotropic etching so that it remains only on the side wall of the gate electrode 404. Next, by adding, for example, approximately  $1 \times 10^{15} \text{ cm}^{-2}$  of the impurities which serve as a donor or an acceptor by ion implantation, a source area 408 and a drain area 409 are formed in a self-aligned manner. The silicon oxide film 407 that remained on the side wall of the gate acts as a stopper at the time of ion implantation and a transistor having a low concentration in the drain end section is formed (See Fig. 4(c)).

Thereafter, a source electrode 410 and a drain electrode 411 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 408 and the drain area 409 according to the usual processes.

However, this method still has problems described below. Firstly, the drain is formed by ion implantation as explained with reference to Fig. 4. Owing to this, the crystal structure is degraded and the trap state density becomes higher in the silicon thin film constituting the drain section.

The trap state density in the silicon film composing the drain is another major parameter which determines the OFF-current in addition to the electric field applied to the drain. Therefore, the effect

of this method is lessened and the decrease in OFF-current is less pronounced.

The second problem is that the number of processes, such as ion implantation, etc., increases greatly.

The structure of the thin film transistor of the present invention effectively lowers the voltage between the gate and the drain during off time, since the gate electrode is formed in the so-called offset structure in which the gate electrode does not overlap the source area or the drain area. Also, the crystal structure in an edge portion of the drain is not degraded. Hence, the value of the OFF-current in the vicinity of a gate voltage of 0 V in a conventional transistor can be maintained for gate voltages less than 0 V according to the invention as shown in Fig. 5. The OFF-characteristics of the thin film transistor can be improved greatly. On the other hand, the ON-current is not significantly decreased as compared to a conventional transistor. The reason therefor is that in a thin film transistor, because the silicon layer of the channel section is thin, the range over which a depletion layer extends is limited and an inversion layer is likely to be formed. Therefore, if the length of the offset section is optimized, a decrease in the ON-current can be suppressed. As a result, it has become possible to provide a thin film transistor having excellent characteristics because of a large ON/OFF ratio.

The present invention will be explained in the following.

Fig. 1 is a cross-sectional view showing the construction of a thin film transistor according to the present invention. A source area 102 and a drain area 103 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, to which an impurity which serves as a donor or an acceptor is added, are formed on an insulating substrate 101 of glass, quartz, sapphire or the like. A channel area 104 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the source area and the drain area in such a manner as to connect these two areas. A source electrode 105 composed of a metal, a transparent electrically-conductive film, etc. is disposed so as to be in contact with the source area 102, and a drain electrode 106 is disposed so as to be in contact with the drain area 103. All of the above is coated with a gate insulation film 107 such as a silicon oxide film, etc. A gate electrode 108 composed of a metal, a transparent electrically-conductive film, etc. is disposed in such a manner as not to cover either the source area 102 or the drain area 103 at the least. The gate insulation film 107 also acts as an interlayer insulation film for maintaining the insulation between interconnections.

### Embodiment 1

Such a thin film transistor can be realized by a process described below. Fig. 6 is a cross-sectional view showing process steps by which a thin film transistor of the present invention is realized. Patterns 602 and 603 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 601 of glass, quartz, sapphire or the like. A pattern 604 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, all of the above is coated with a gate insulation film 605 such as a silicon oxide film, etc. Formed thereon is a gate electrode 606 composed of a metal, a transparent electrically-conductive film, a polycrystalline silicon film to which an impurity which serves as a donor or an acceptor is added, etc. (See Fig. 6(a)).

Next, an insulation film 607, for example, a silicon oxide film, is formed on all of the above. By adding an impurity which serves as a donor or an acceptor by ion implantation, a source area 608 and a drain area 609 are formed in a self-aligned manner with respect to the gate electrode. At this time, the silicon oxide film 607 formed on the side wall of the gate is effectively a thick film when seen from a vertical direction and serves as a stopper for ions implanted. As a result, a transistor having an offset structure is formed (See Fig. 6(b)).

Thereafter, a source electrode 610 and a drain electrode 611 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 608 and the drain area 609 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 6(c)).

### Embodiment 2

Fig. 7 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized. Patterns 702 and 703 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 701 of glass, quartz, sapphire or the like. A pattern 704 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, all of the above is coated with a gate insulation film 705 such as a silicon oxide film, etc. Formed thereon is a gate electrode 706 composed of a metal, a transparent electrically-conductive film, a poly-

crystalline silicon film to which an impurity is added, etc. (See Fig. 7(a)).

Next, after an insulation film 707 of, for example, silicon oxide, has been formed on all of the above, this insulation film 707 is etched by anisotropic etching so that it remains only on the side wall of the gate electrode 706. Next, by adding an impurity which serves as a donor or an acceptor by ion implantation, a self-aligned source area 708 and a self-aligned drain area 709 are formed. At this time, the silicon oxide film 707 that remained on the side wall of the gate serves as a stopper for ions implanted. As a result, a transistor having an offset structure is formed (See Fig. 7(b)).

Thereafter, a source electrode 710 and a drain electrode 711 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 708 and the drain area 709 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 7(c)).

### Embodiment 3

Fig. 8 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized.

Patterns 802 and 803 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 801 of glass, quartz, sapphire or the like. A pattern 804 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, all of the above is coated with a gate insulation film 805 such as a silicon oxide film, etc. Next, formed in turn thereon is an electrically conductive film 806 which serves as a gate electrode (See Fig. 8(a)). Next, a resist pattern 807 is formed on the electrically conductive film 806 by using a photo etching technique. With this pattern as a mask, the electrically conductive film 806 is selectively etched in such a way that it becomes small relative to the resist pattern, and a gate electrode 808 is formed. By adding an impurity which serves as a donor or an acceptor by ion implantation, a self-aligned source area 809 and a self-aligned drain area 810 are formed. Then, the resist pattern 807 is removed (See Fig. 8(b)).

Thereafter, a source electrode 811 and a drain electrode 812 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 809 and the drain area 810 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 8(c)).

#### Embodiment 4

Fig. 9 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized.

Patterns 902 and 903 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 901 of glass, quartz, sapphire or the like. A pattern 904 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, all of the above is coated with a gate insulation film 905 such as a silicon oxide film, etc. Next, formed in turn thereon is an electrically conductive film 906 which serves as a gate electrode (See Fig. 9(a)).

Next, a resist pattern 907 is formed on the electrically conductive film 906 by using a photo etching technique. With this pattern as a mask, the electrically conductive film 906 is selectively etched, and a gate electrode 908 is formed. Then, by adding an impurity which serves as a donor or an acceptor by ion implantation, a self-aligned source area 909 and a self-aligned drain area 910 are formed with respect to the gate electrode. Then, the gate electrode 908 is etched in such a way that it becomes small relative to the resist pattern. Thereafter, the resist pattern 907 is removed (See Fig. 9(b)).

Thereafter, a source electrode 911 and a drain electrode 912 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 909 and the drain area 910 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 9(c)).

#### Embodiment 5

Fig. 10 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized.

Patterns 1002 and 1003 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 1001 of glass, quartz, sapphire or the like. A pattern 1004 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, formed in turn thereon are a gate insulation film 1005 such as a silicon oxide film, etc., an electrically conductive film 1006 which serves as a gate electrode, and a film 1007 such as a silicon oxide film, etc. (See Fig. 10(a)).

Next, a resist pattern 1008 is formed on the silicon oxide film 1007 by using a photo etching technique. With this pattern as a mask, the silicon oxide film 1007 is selectively etched (See Fig. 10(b)).

Thereafter, the resist pattern 1008 is removed. Then, with the silicon oxide film 1007 as a mask, the electrically conductive film 1006 is selectively etched in such a way that it becomes small relative to the silicon oxide film pattern 1007. Thus, a gate electrode 1009 is formed. Then, by adding an impurity which serves as a donor or an acceptor by ion implantation, a source area 1010 and a drain area 1011 are formed in a self-aligned manner with respect to the gate electrode (See Fig. 10(c)).

Thereafter, a source electrode 1012 and a drain electrode 1013 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 1010 and the drain area 1011 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 10(d)).

#### Embodiment 6

Fig. 11 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized.

Patterns 1102 and 1103 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 1101 of glass, quartz, sapphire or the like. A pattern 1104 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas.

Next, formed in turn on all of the above are a gate insulation film 1105 such as a silicon oxide film, etc., an electrically conductive film 1106 which serves as a gate electrode, and a film 1107 such as a silicon oxide film, etc. (See Fig. 11(a)).

Next, a resist pattern 1108 is formed on the silicon oxide film 1107 by using a photo etching technique. With this pattern as a mask, the silicon oxide film 1107 is selectively etched (See Fig. 11(b)).

Thereafter, the resist pattern 1108 is removed. Then, with the silicon oxide film 1107 as a mask, the electrically conductive film 1106 is selectively etched and a gate electrode 1109 is formed. Then, by adding an impurity which serves as a donor or an acceptor by ion implantation, a self-aligned source area 1110 and a self-aligned drain area 1111 are formed. Next, the gate electrode 1109 is

selectively etched in such a way that the gate electrode 1109 becomes small relative to the silicon oxide film 1107 (See Fig. 11(c)).

Thereafter, a source electrode 1112 and a drain electrode 1113 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 1110 and the drain area 1111 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 11(d)).

#### Embodiment 7

Fig. 12 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized.

Patterns 1202 and 1203 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 1201 of glass, quartz, sapphire or the like. A pattern 1204 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, formed in turn on all of the above are a gate insulation film 1205 such as a silicon oxide film, etc. and an electrically conductive film 1206 which serves as a gate electrode (See. Fig. 12(a)).

Next, a resist pattern 1207 is formed on the electrically conductive film 1206 by using a photo etching technique. With this pattern as a mask, the electrically conductive film 1208 is selectively etched and a gate electrode 1208 is formed (see Fig. 12(b)).

Then, by adding an impurity which serves as a donor or an acceptor by ion implantation, a self-aligned source area 1209 and a self-aligned drain area 1210 are formed. Next, the gate electrode 1208 is selectively etched so as to be small (See Fig. 12(c)).

Thereafter, a source electrode 1211 and a drain electrode 1212 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 1209 and the drain area 1210 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 12(d)).

#### Embodiment 8

Fig. 13 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized.

5 Patterns 1302 and 1303 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 1301 of glass, quartz, sapphire or the like. A pattern 1304 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, formed in turn 10 on all of the above are a gate insulation film 1305 such as a silicon oxide film, etc., an electrically conductive film 1306 which serves as a gate electrode, and a film 1307 such as a silicon oxide film, etc. (See Fig. 13(a)).

15 Next, a resist pattern 1308 is formed on the silicon oxide film 1307 by using a photo etching technique. With this pattern as a mask, the silicon oxide film 1307 is selectively etched (See Fig. 13(b)).

20 Then, with the silicon oxide film 1107 as a mask, the electrically conductive film 1106 is selectively etched and a gate electrode 1309 is formed. Thereafter, the resist pattern 1307 is removed. Then, after an insulation film 1310 such as a silicon oxide film, etc. has been formed on all of the

25 above, this silicon oxide film 1310 is etched by anisotropic etching so that it remains on the side wall of the gate electrode 1309. At this time, the gate electrode 1309 is coated with the silicon oxide films 1307 and 1310. Then, by adding an impurity which serves as a donor or an acceptor by ion implantation, a self-aligned source area 1311 and a self aligned drain area 1312 are formed (See Fig. 13(c)).

30 35 Thereafter, a source electrode 1313 and a drain electrode 1314 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 1311 and the drain area 1312 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 13(d)).

#### Embodiment 9

40 45 Fig. 14 is a cross-sectional view showing the process steps of another embodiment by which a thin film transistor of the present invention is realized.

A pattern 1402 which is composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed on an insulating substrat 1401 of glass, quartz, sapphire or the like. Next, all of th above is coated with a gate insulation film 1403 such as a silicon oxide film, etc. From d thereon is a gate electrod 1404 composed of a metal, an electrically conductive film, a polycrystalline silicon film to which an impurity is

added, etc. (See Fig. 14(a)).

Next, after an insulation film 1405, for example, a silicon oxide film, has been formed on all of the above, the insulation film 1405 and the gate insulation film 1403 are selectively etched so that at least a part of the pattern 1402 is exposed. Next, patterns 1406 and 1407 which are composed of a polycrystalline silicon film, to which an impurity is added, are formed in a manner as to connect to the pattern 1402. These patterns act as source and drain area, respectively.

Thereafter, a source electrode 1408 and a drain electrode 1409 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 1406 and the drain area 1407 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 14(c)).

#### Embodiment 10

Fig. 15 is a cross-sectional view showing process steps of another embodiment by which a thin film transistor of the present invention is realized.

Patterns 1502 and 1503 which are composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, are formed on an insulating substrate 1501 of glass, quartz, sapphire or the like. A pattern 1504 composed of a silicon thin film, of such as polycrystalline silicon or amorphous silicon, is disposed so as to be in contact with the top side of the two areas in such a manner as to connect these two areas. Next, all of the above is coated with a gate insulation film 1505 such as a silicon oxide film, etc. Formed thereon is a gate electrode 1506 composed of a metal, an electrically conductive film, a polycrystalline to which an impurity is added, etc. (See Fig. 15(a)).

Then, an insulation film 1507, for example, a silicon oxide film, etc. is formed on all of the above. Next, a resist pattern 1508 is formed thereon by using a photo etching technique. With this pattern as a mask, by adding an impurity which serves as a donor or an acceptor to at least a part of each of the patterns 1502 and 1503 by ion implantation, a source area 1509 and a drain area 1510 are formed (See Fig. 15(b)).

Thereafter, the resist pattern 1508 is removed. A source electrode 1511 and a drain electrode 1512 which are composed of a metal, a transparent electrically-conductive film, etc. are respectively connected to the source area 1509 and the drain area 1510 according to the usual processes. Thus, a thin film transistor according to the present invention is completed (See Fig. 15(c)).

In the above, embodiments for realizing the present invention have been explained. The

present invention can be realized by using materials other than those mentioned above without departing from the spirit and scope of the present invention. The embodiments have been explained chiefly by showing a structure in which the thickness of silicon films of at least a part of a source area and a drain area is different from that of a channel section. However, as shown in Fig. 16, a thin film transistor having a structure in which the thickness of silicon films of, for example, the source area 1601 and the drain area 1602, is the same as that of the channel area 1603, may be used without departing from the spirit and scope of the present invention. In Fig. 16, 1605 is a gate insulation film, 1604 a gate electrode, 1606 a source electrode, 1607 a drain electrode and 1608 a substrate.

As has been explained above, with the thin film transistor of the present invention, it is possible to reduce the OFF-current dramatically without reducing the ON-current. This thin film transistor is a breakthrough invention which paves the way particularly for an integrated driver built-in a large type liquid crystal display. In addition, a considerable improvement in the performance of the display and a reduction in costs thereof can be expected when a conventional thin film transistor is replaced with the thin film transistor of the present invention. For example, in a conventional liquid crystal display, since the OFF-current of a thin film transistor used in the pixel section thereof is large, transistors are connected in series in order to reduce the OFF-current. However, the above does not have to be done if the thin film transistor of the present invention is used and therefore the yield and the picture quality of the display can be enhanced.

As set forth hereinabove, the present invention can be used for all applications for which thin film transistors are used, such as image sensors, liquid crystal displays, etc. The present invention makes a great contribution toward improving the performance of the above devices and reducing the costs thereof.

#### Claims

1. A thin film transistor, comprising:  
a source area (102) and a drain area (103) which are composed of a silicon thin film to which an impurity which serves as a donor or an acceptor is added;  
a channel area (104) composed of the silicon thin film formed between said source area and said drain area in contact with said source area and said drain area;  
a gate insulation film (107) formed in such a manner as to cover said source area, said drain area, and said channel area; and

a gate electrode (108) disposed on said gate insulation film, wherein said gate electrode does not overlap said source area or said drain area.

2. A thin film transistor as claimed in claim 1, wherein said gate electrode does overlap neither said source area nor said drain area.

3. A thin film transistor as claimed in claim 1, wherein said gate electrode does not overlap said drain area.

4. A method of manufacturing the thin film transistor as claimed in claim 1, comprising the steps of:

- forming an element area by selectively etching a silicon thin film;
- forming in turn said gate insulation film and an electrically conductive film for said gate electrode on said silicon thin film;
- forming said gate electrode by selectively etching said electrically conductive film; and
- forming said source area and said drain area in a self-aligned manner by adding an impurity which serves as a donor or an acceptor after an insulation film has been formed on said gate electrode.

5. A method of manufacturing the thin film transistor as claimed in claim 1, comprising the steps of:

- forming an element area by selectively etching a silicon thin film;
- forming in turn said gate insulation film and an electrically conductive film for said gate electrode on said silicon thin film;
- forming said gate electrode by selectively etching said electrically conductive film;
- forming an insulation film on said gate electrode by anisotropic etching in such a manner as to remain on the side wall of said gate electrode at the least; and
- forming said source area and said drain area in a self-aligned manner by adding an impurity which serves as a donor or an acceptor after an insulation film has been formed on said gate electrode.

6. A method of manufacturing the thin film transistor as claimed in claim 1, comprising the steps of:

- forming an element area by selectively etching a silicon thin film;
- forming in turn said gate insulation film and an electrically conductive film for said gate electrode on said silicon thin film;
- forming said gate electrode by selectively

5 etching said electrically conductive film with a pattern composed of a mask material as a mask in such a way that it becomes small relative to the pattern composed of the mask material; and

10 forming said source area and said drain area in a self-aligned manner by adding an impurity which serves as a donor or an acceptor after an insulation film has been formed on said gate electrode.

15 7. A method of manufacturing the thin film transistor as claimed in claim 1, comprising the steps of:

- forming an element area by selectively etching a silicon thin film;
- forming in turn said gate insulation film and an electrically conductive film for said gate electrode on said silicon thin film;
- 20 forming said gate electrode by selectively etching said electrically conductive film with a pattern composed of a mask material as a mask;
- forming said source area and said drain area in a self-aligned manner by adding an impurity which serves as a donor or an acceptor after an insulation film has been formed; and making said gate electrode small relative to the pattern composed of the mask material.

25 30 8. A method of manufacturing the thin film transistor as claimed in claim 1, comprising the steps of:

- forming an element area by selectively etching a silicon thin film;
- 35 forming in turn said gate insulation film and an electrically conductive film for said gate electrode on said silicon thin film;
- forming said gate electrode by selectively etching said electrically conductive film with a pattern composed of a mask material as a mask;
- removing said pattern composed of the mask material;
- forming said source area and said drain area in a self-aligned manner by adding an impurity which serves as a donor or an acceptor after an insulation film has been formed; and

40 45 50 making said gate electrode small relative to the pattern composed of the mask material.

55 9. A method of manufacturing the thin film transistor in which said gate electrode does not overlap said source area or said drain area as claimed in claim 1, comprising the steps of:

- forming an element area by selectively etching a silicon thin film;

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forming in turn said gate insulation film, an electrically conductive film for said gate electrode, and a first insulation film on said silicon thin film;

forming said gate electrode having a construction in which an insulation film remains on top of the gate electrode area only by selectively etching in turn said first insulation film and said electrically conductive film;

forming a second insulation film on said gate electrode;

etching said second insulation film by anisotropic etching in such a manner as to remain on the side wall of said gate electrode at the least; and

forming said source area and said drain area by forming a silicon film, to which an impurity which serves as a donor or an acceptor is added, on a part of said element area.

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10. A method of manufacturing the thin film transistor in which said gate electrode does not overlap said source area or said drain area as claimed in claim 1, comprising the steps of:

forming an element area by selectively etching a silicon thin film;

forming in turn said gate insulation film and an electrically conductive film for said gate electrode on said silicon thin film;

forming said gate electrode by selectively etching said electrically conductive film;

forming a mask pattern such as to cover said gate electrode which overlaps the channel area at the least; and

forming said source area and said drain area by adding an impurity which serves as a donor or an acceptor with said mask pattern as a mask.

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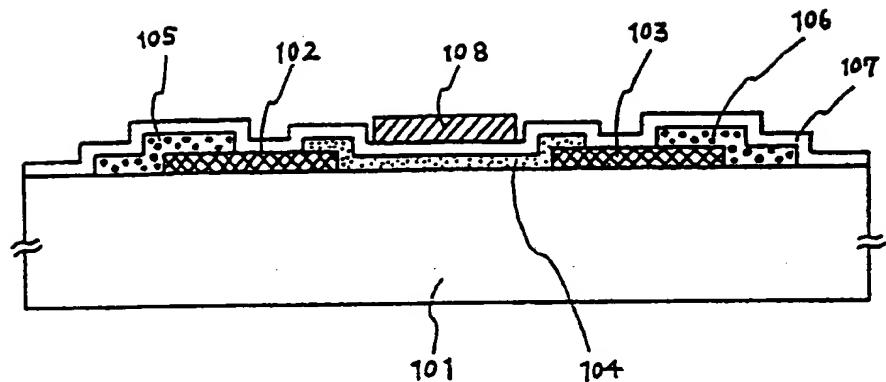


FIG. 1

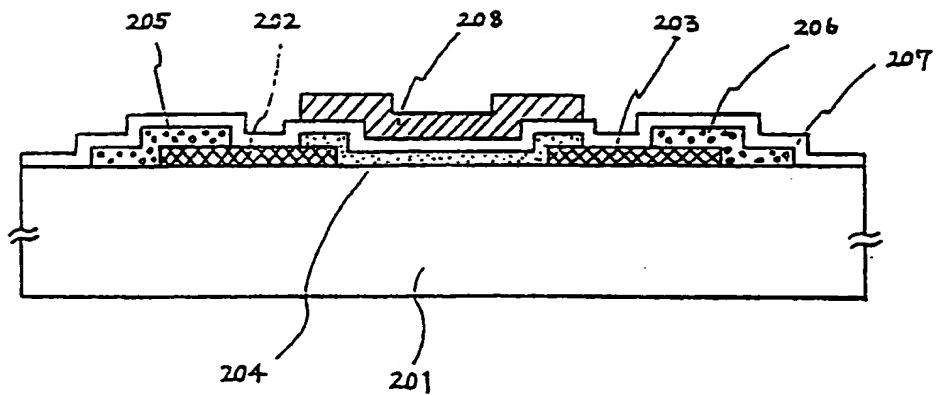
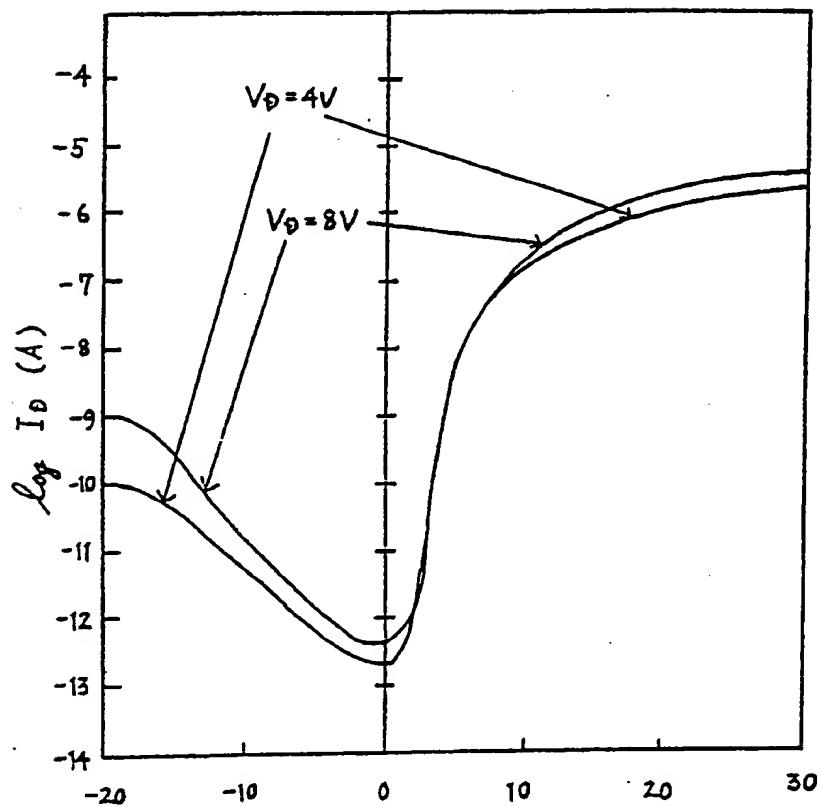


FIG. 2

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$V_{gs}$  (Volt)

FIG. 3

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FIG. 4(a)

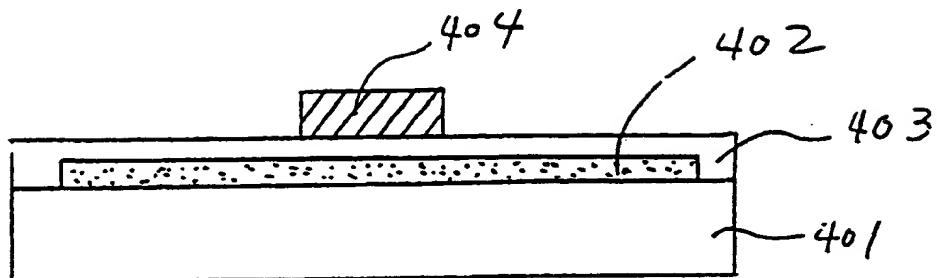


FIG. 4(b)

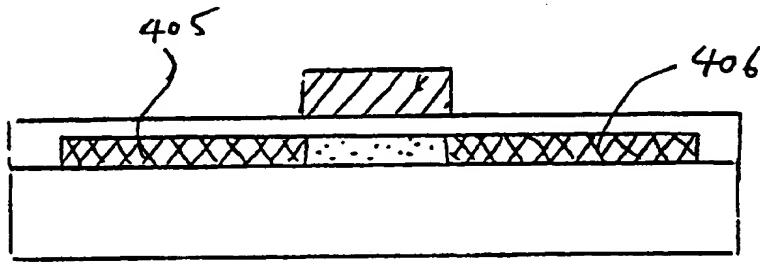


FIG. 4(c)

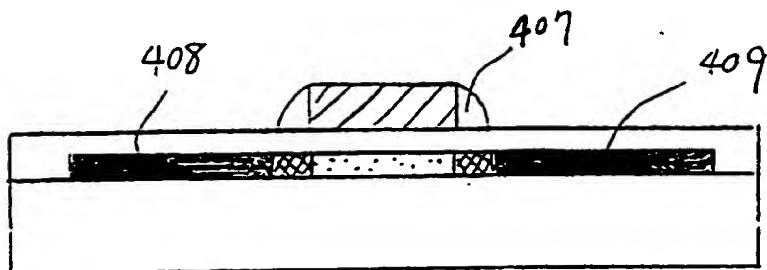
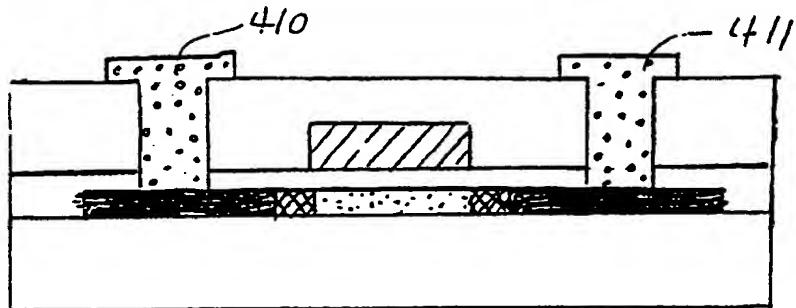


FIG. 4(d)



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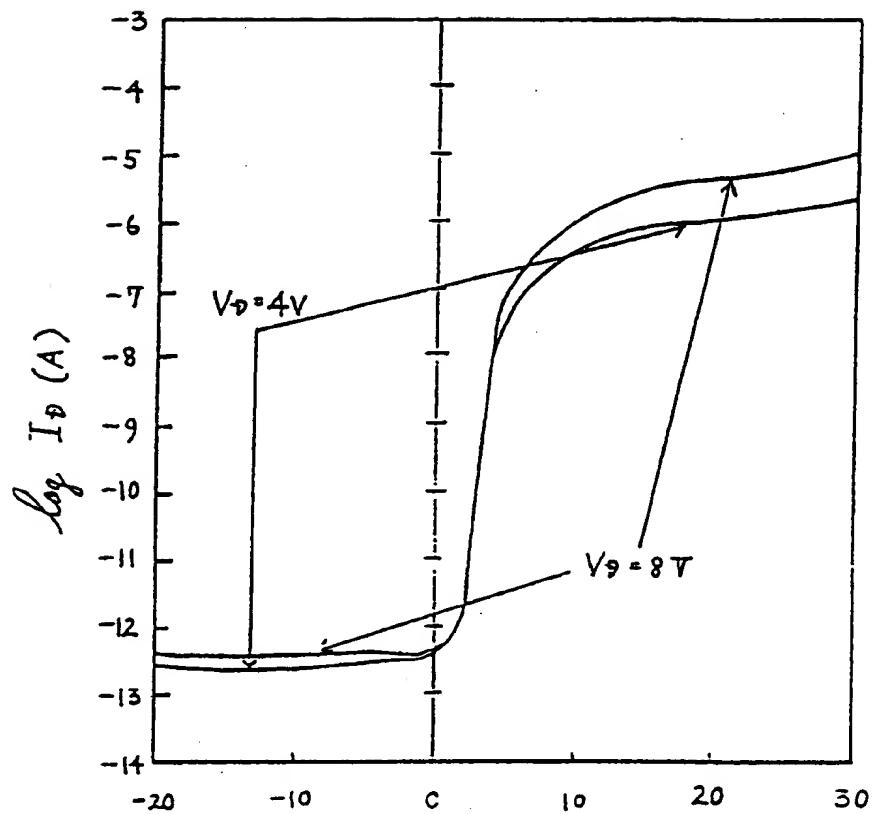
 $V_{gs}$  (Volt)

FIG. 5

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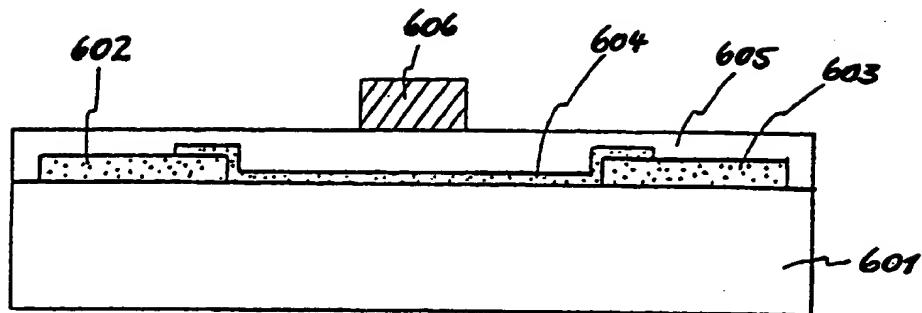


FIG. 6 (a)

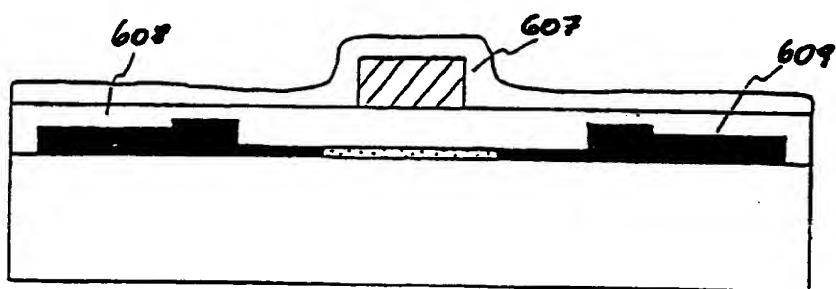


FIG. 6 (b)

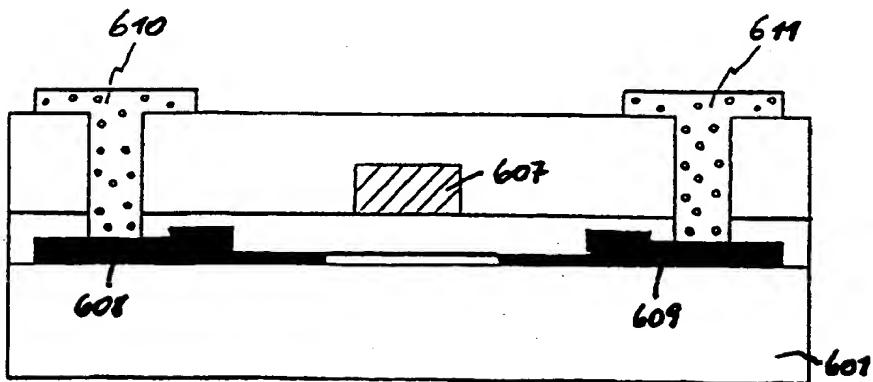


FIG. 6 (c)

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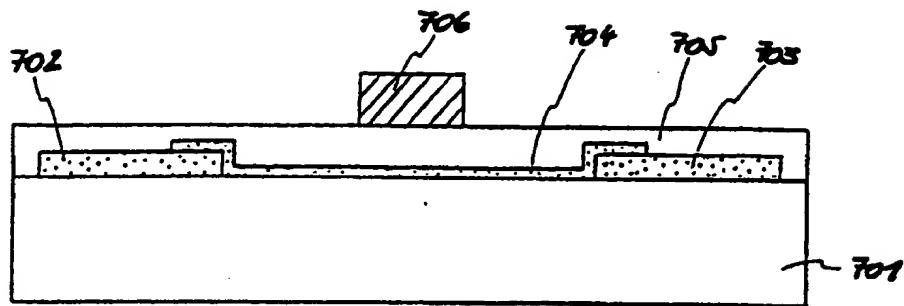


FIG. 7(a)

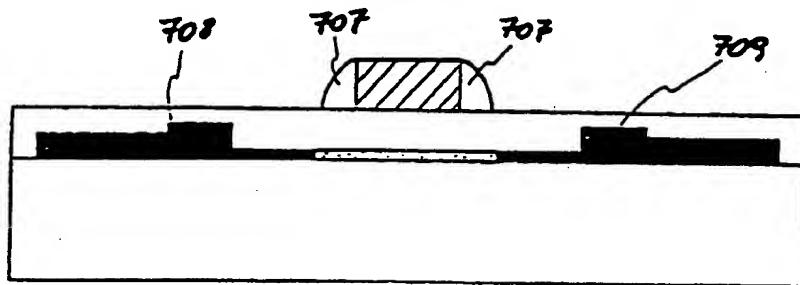


FIG. 7(b)

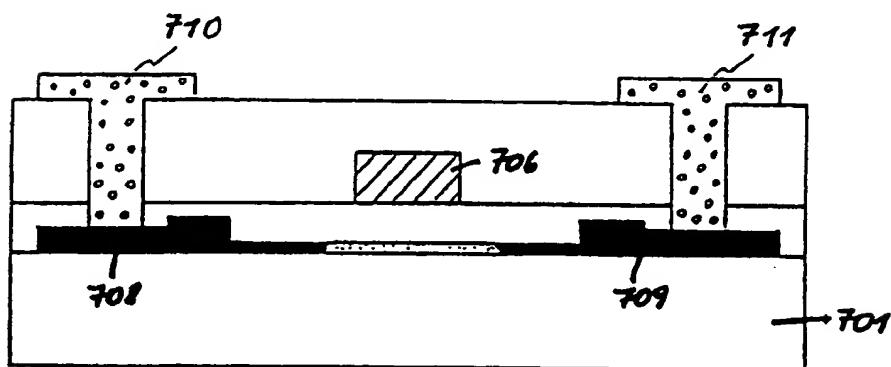


FIG. 7(c)

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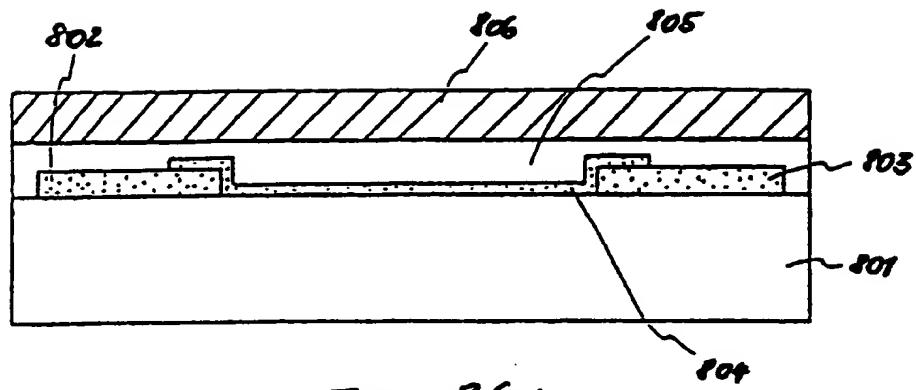


FIG. 8(a)

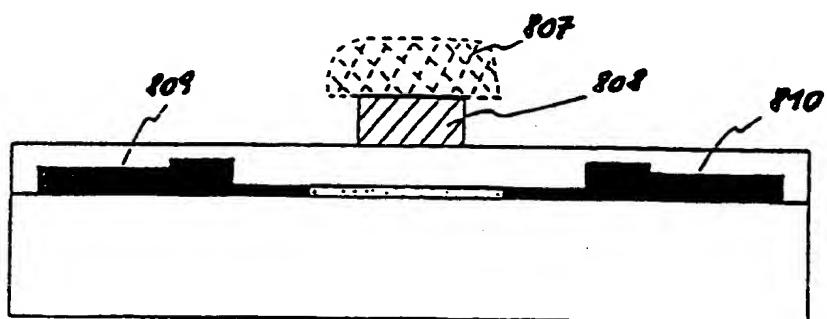


FIG. 8(b)

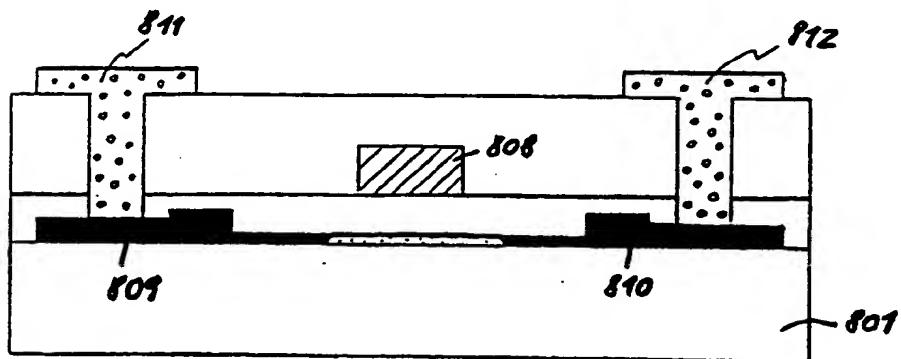


FIG. 8(c)

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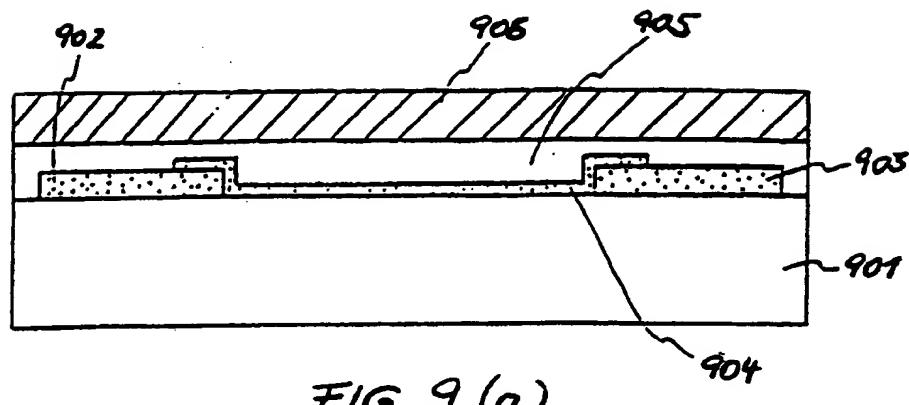


FIG. 9 (a)

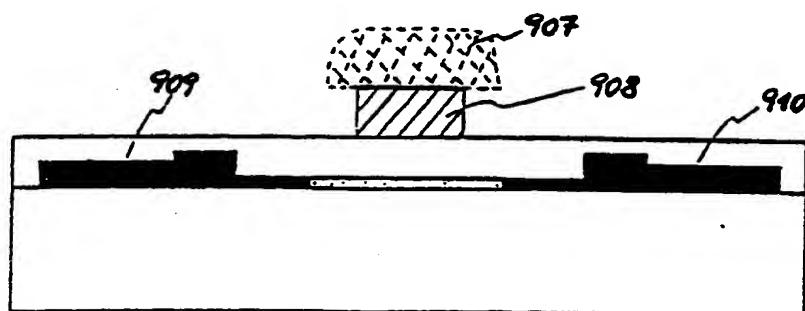


FIG. 9 (b)

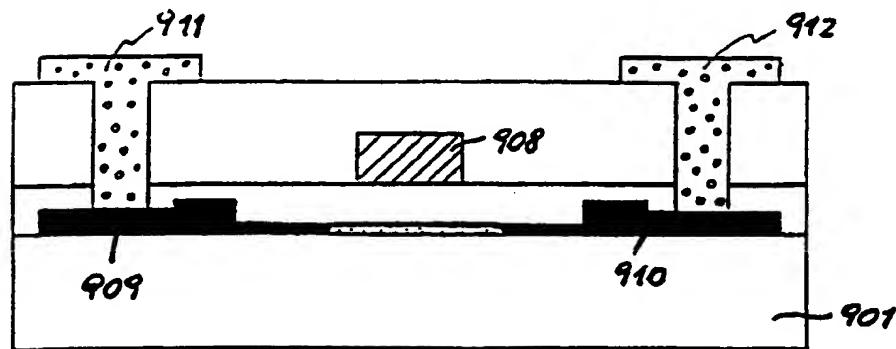


FIG. 9(c)

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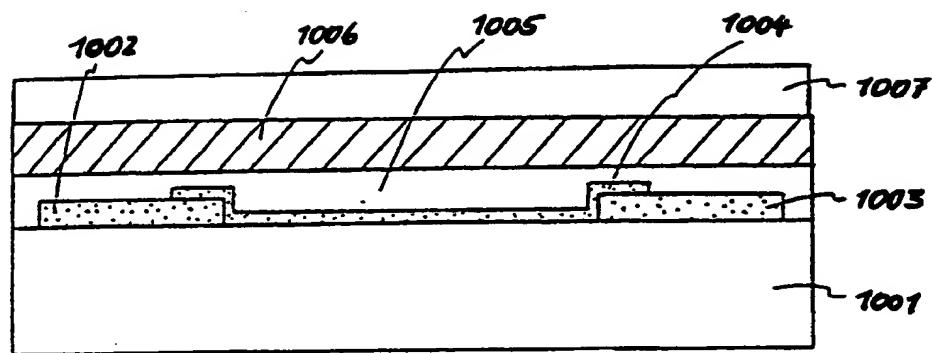


FIG. 10 (a)

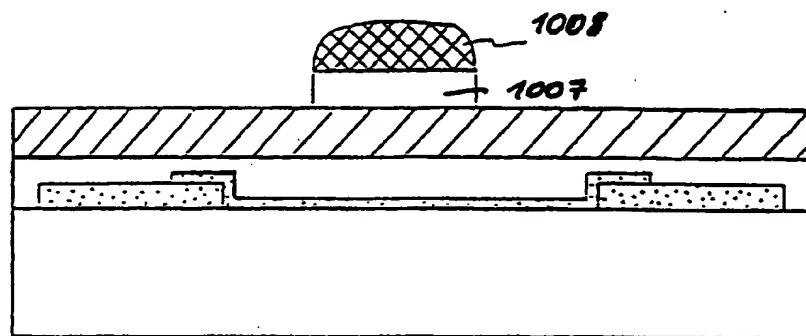


FIG. 10 (b)

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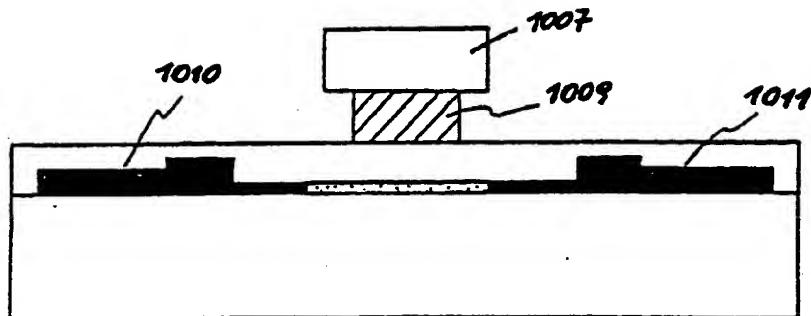


FIG. 10 (c)

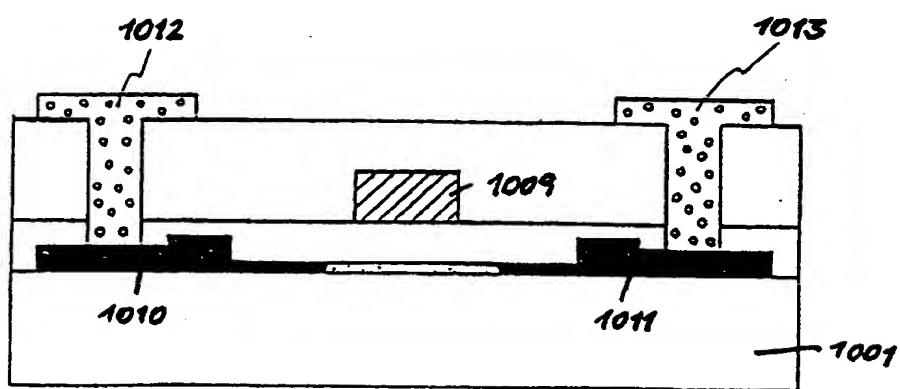


FIG. 10 (d)

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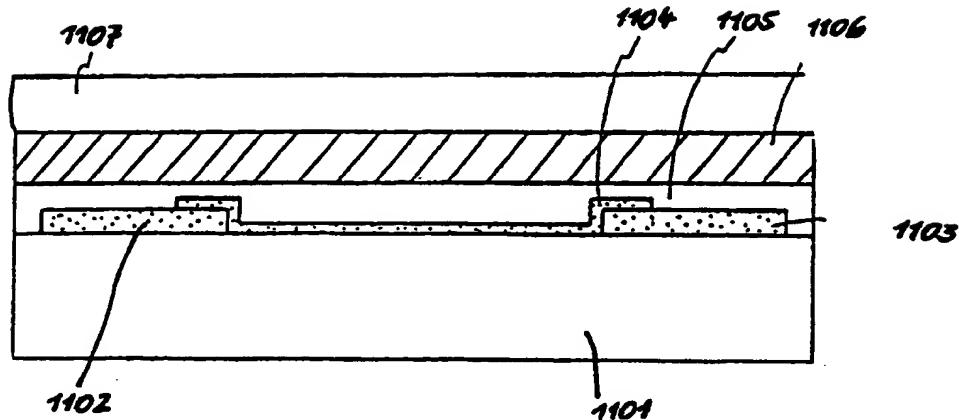


FIG. 11 (a)

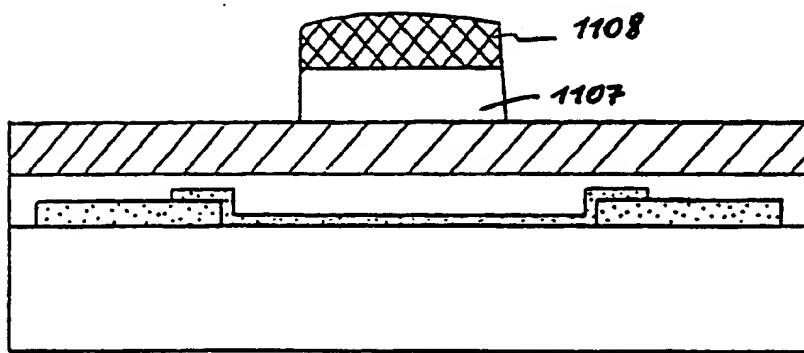


FIG. 11 (b)

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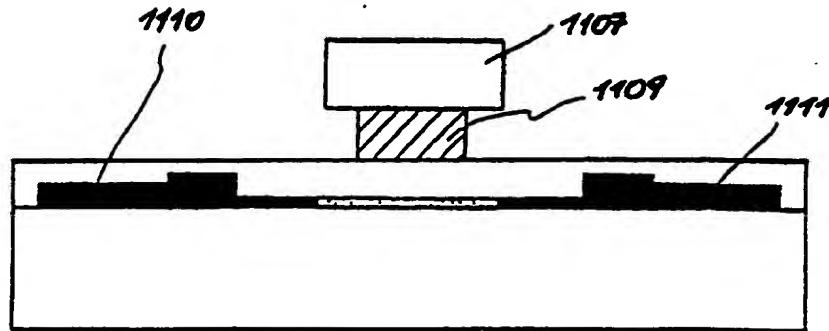


FIG. 11(c)

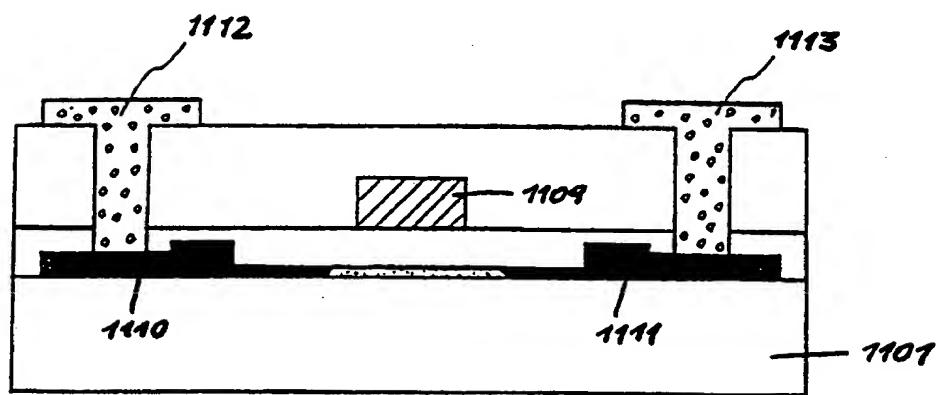


FIG. 11(d)

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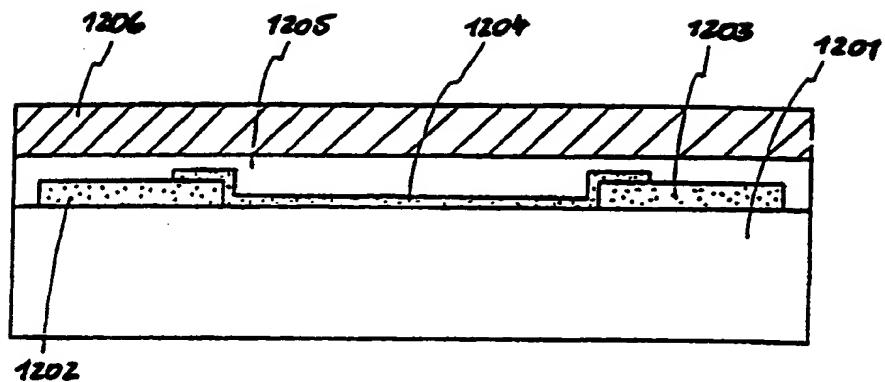


FIG. 12 (a)

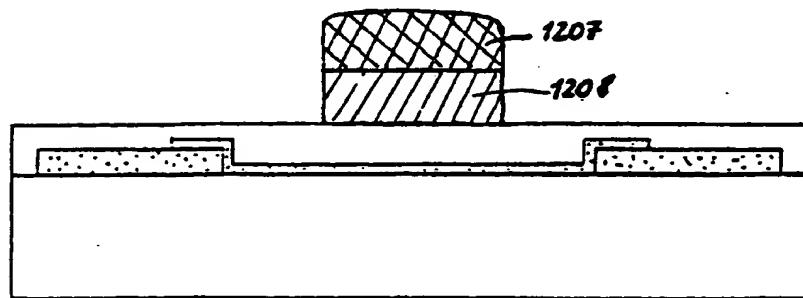


FIG. 12 (b)

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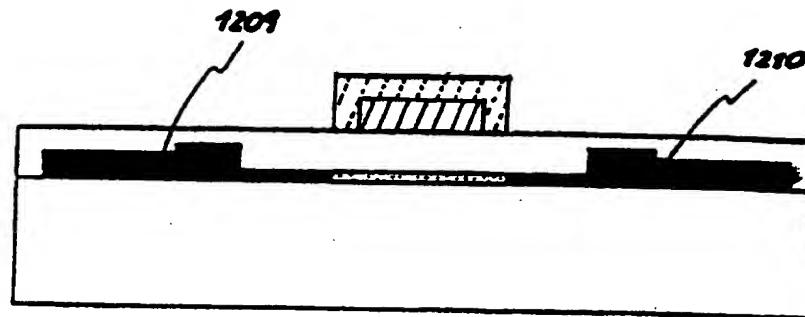


FIG. 12 (c)

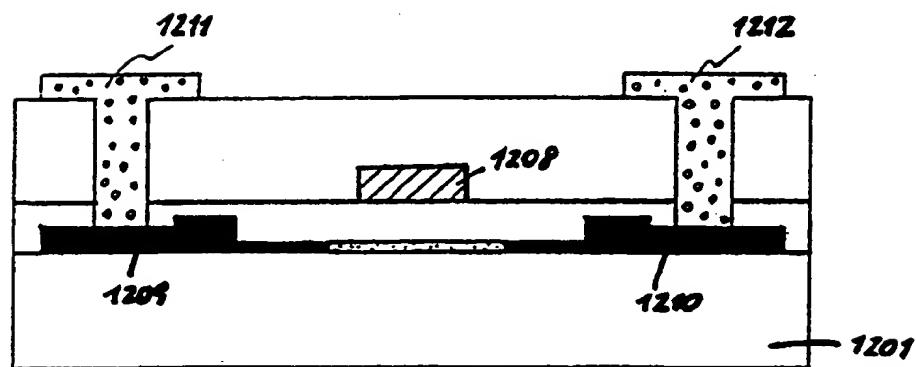


FIG. 12 (d)

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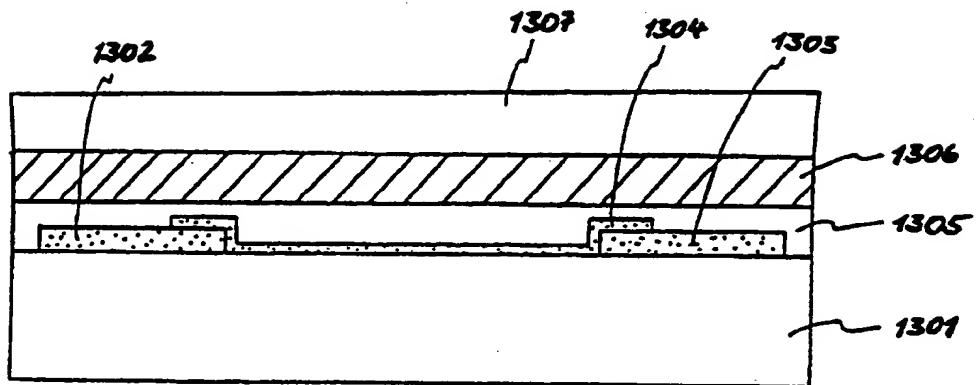


FIG. 13 (a)

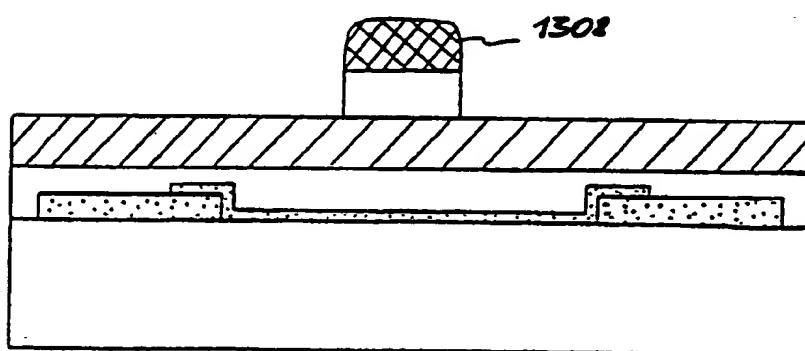


FIG. 13 (b)

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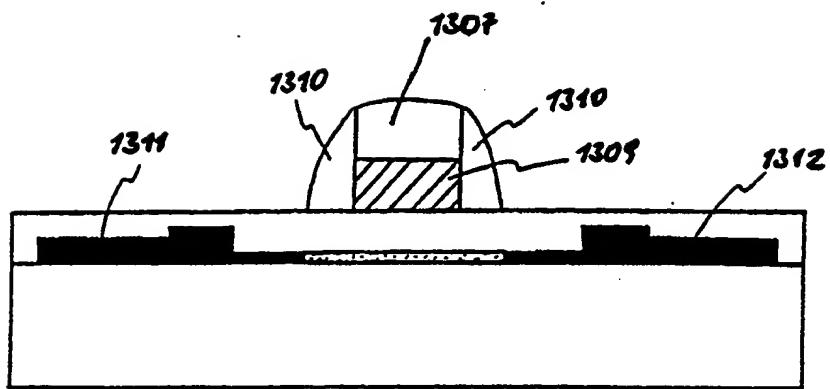


FIG. 13 (c)

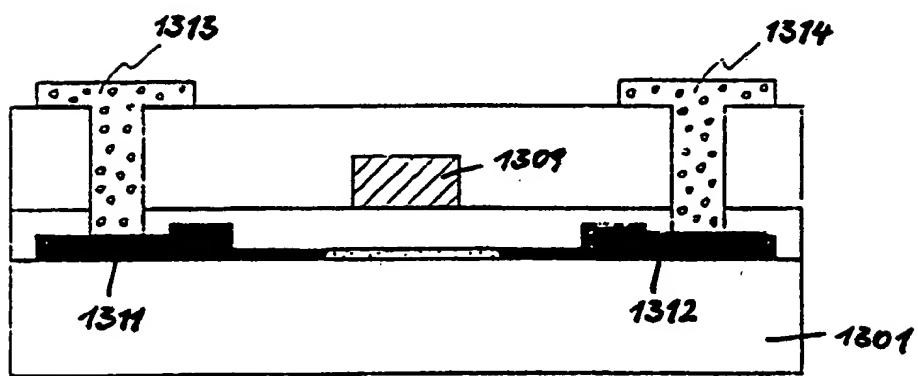


FIG. 13 (d)

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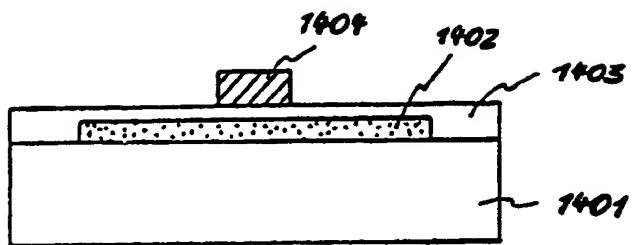


FIG. 14 (a)

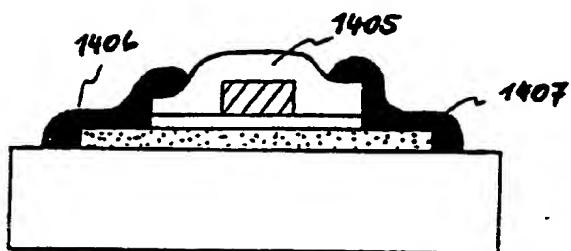


FIG. 14 (b)

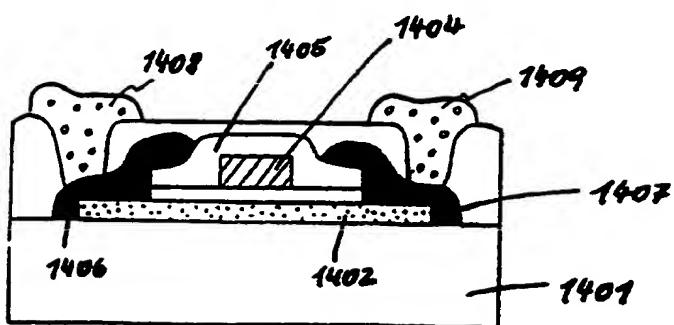


FIG. 14 (c)

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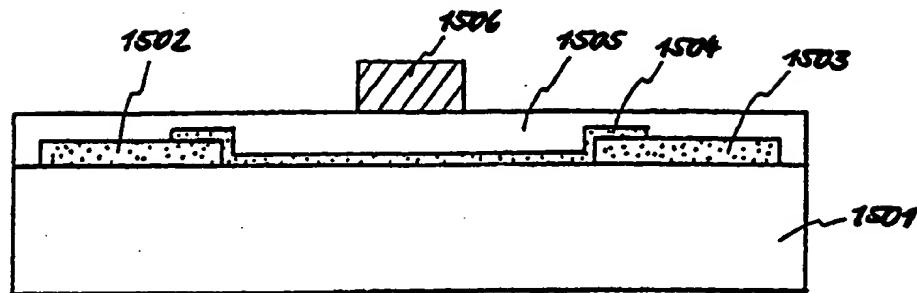


FIG. 15 (a)

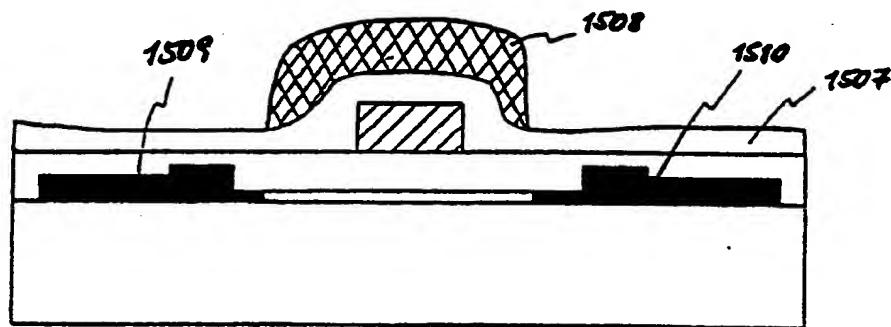


FIG. 15 (b)

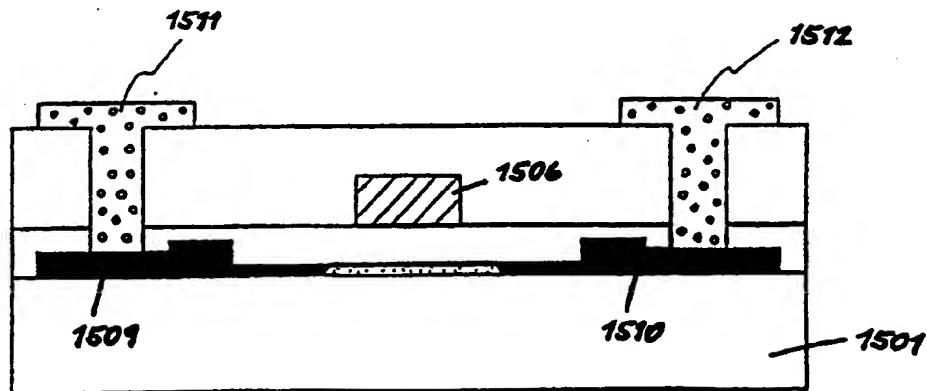


FIG. 15 (c)

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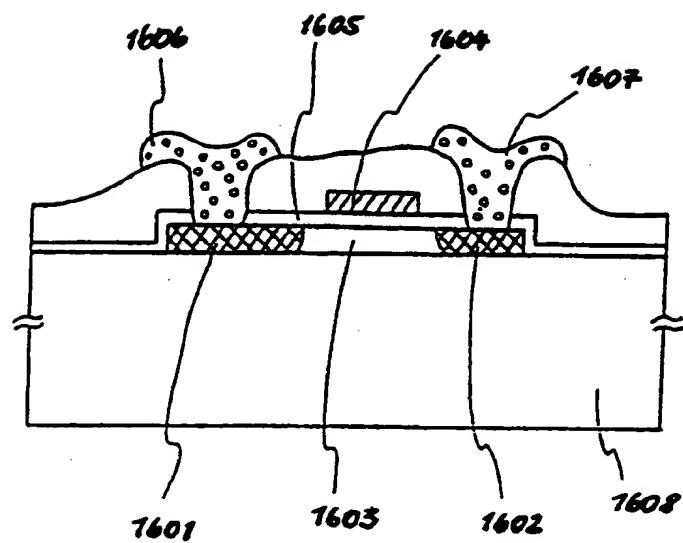


FIG. 16



European  
Patent Office

EUROPEAN SEARCH  
REPORT

Application Number

EP 91 10 9110

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.8)		
X,Y	PATENT ABSTRACTS OF JAPAN vol. 013, no. 321 (E-790) 20 July 1989, & JP-A-01 089464 (TOSHIBA CORP) 03 April 1989, * the whole document * ----- US-A-4 751 196 (MOTOROLA INC.) * column 3, line 66 - column 4, line 47; figure 4 * -----	1,2,5,1,4, 6-9	H 01 L 29/784		
X	PATENT ABSTRACTS OF JAPAN vol. 007, no. 226 (E-202) 07 October 1983, & JP-A-58 115864 (NIPPON DENSHIN DENWA KOSHA) 09 July 1983, * the whole document *	1,2			
X	EP-A-0 399 737 (XEROX CORPORATION) * abstract; figure 2 *	1,10			
Y	EP-A-0 159 617 (SIEMENS AKTIENGESELLSCHAFT) * abstract; figures *	1,4			
Y	US-A-4 198 250 (INTEL CORPORATION) * abstract; figures *	1,6	TECHNICAL FIELDS SEARCHED (Int. CL8)		
Y	EP-A-0 195 607 (FUJITSU LIMITED) * column 5, lines 14 - 44; figures 7A-7D *	1,7	H 01 L		
Y,Y	EP-A-0 190 928 (KABUSHIKI KAISHA TOSHIBA) * page 3, line 23 - page 4, line 19; figures 2, 8 ** page 13, line 10 - page 16, line 7; figure 7 *	1,8,1,9			
The present search report has been drawn up for all claims					
Place of search	Date of completion of search	Examiner			
The Hague	29 August 91	MIMOUN B.J.			
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D: document cited in the application					
L: document cited for other reasons					
I: member of the same patent family, corresponding document					